IN THE CLAIMS

1. (Withdrawn) In a communications system, a method for non-causal channel equalization, the method comprising:

receiving a non-return to zero (NRZ) data stream input;

comparing a first bit estimate in the data stream to a second bit value received prior to the first bit;

comparing the first bit estimate to a third bit value received subsequent to the first bit; and,

in response to the comparisons, determining the value of the first bit.

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2. (Withdrawn) The method of claim 1 further comprising:

establishing a first threshold (V1) to distinguish a high probability "1" first bit estimate;

establishing a second threshold (V0) to distinguish a high probability "0" first bit estimate;

establishing a third threshold (Vopt) to distinguish first bit estimates between the first and second thresholds;

supplying the first bit estimate for comparison in response to distinguishing the NRZ data stream input at the first, second, and third thresholds.

3. (Withdrawn) The method of claim 2 wherein establishing a third threshold (Vopt) to distinguish first bit estimates between the first and second thresholds includes:

distinguishing NRZ data stream inputs below first threshold and above the third threshold as a "0" if both the second and third bits are "1" values, as a "1" if only one of the second and third bits is a "1" value, and as "1" if both the second and third bits are a "0" value; and,

distinguishing NRZ data stream inputs above the second threshold and below the third threshold as a "1" if both the second and third bits are a "0" value, as a "0" if only one of the second and third values is a "0" value, and as a "0" if both the second and third bits are a "1" value.

4. (Withdrawn) The method of claim 3 wherein receiving a non-return to zero data stream includes receiving a non-return to zero data stream encoded with forward error correction (FEC);

the method further comprising:

following the determination of the first bit values, FEC decoding the first bit values; and,

using the FEC corrections of the first bit values to adjust the first, second, and third threshold values.

5. (Withdrawn) The method of claim 4 wherein using the FEC corrections of the first bit values to adjust the first, second, and third threshold values includes:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "1" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "1" values; and,

adjusting the first threshold (V1) in response to corrections tracked when the second and third bits are both "1" values.

6. (Withdrawn) The method of claim 5 wherein using the FEC corrections of the data stream to adjust the first, second, and third threshold values includes:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "0" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "0" values; and,

adjusting the second threshold (V0) in response to corrections tracked when the second and third bits are both "0" values.

7. (Withdrawn) The method of claim 6 wherein using the FEC corrections of the data stream to adjust the first, second, and third threshold values includes:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and only one of the second and third bits is a "1" value; and,

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and only of the second and third bits is a "1" value; and,

adjusting the third threshold (Vopt) in response to corrections tracked when only one of the second or third bit values is a "1" value.

8. (Withdrawn)The method of claim 6 wherein using the FEC corrections of the data stream to adjust the first, second, and third threshold values includes:

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value; and,

adjusting the third threshold (Vopt) in response to corrections tracked when the first bit is determined to be a "1" value.

9. (Withdrawn)The method of claim 3 further comprising:

tracking the NRZ data stream inputs when the second bit value equals the third bit value;

maintaining long-term averages of the tracked NRZ data stream inputs; and,

adjusting the first and second thresholds in response to the long-term averages.

10. (Withdrawn)The method of claim 9 wherein tracking the NRZ data stream inputs when the second bit value equals the third bit value includes:

tracking the NRZ data stream inputs when the second and third bits both have "1" values; and,

tracking the NRZ data stream inputs the second and third bits have "0" values.

11. (Withdrawn)The method of claim 10 wherein maintaining long-term averages of the NRZ data stream inputs includes:

creating a first average of the NRZ data stream inputs when the second and third bits are both "1" values; and,

creating a second average of the NRZ data stream inputs when the second and third bits are both "0" values.

12. (Withdrawn)The method of claim 11 wherein adjusting the first and second thresholds in response to the long-term averages includes:

adjusting the first threshold (V1) in response to the first average; and,

adjusting the second threshold (V0) in response to the second average.

13. (Withdrawn)The method of claim 12 further comprising:

adjusting the third threshold (Vopt) in response to adjusting the first (V1) and second (V0) thresholds.

14. (Withdrawn)The method of claim 13 wherein adjusting the third threshold (Vopt) in response to adjusting the first (V1) and second (V0) thresholds includes setting the third threshold approximately midway between the first and second thresholds.

15. (Withdrawn)The method of claim 9 further comprising:

measuring the average NRZ data stream input voltage; and,

setting the third threshold in response to the measured average.

16. (Withdrawn)The method of claim 3 further comprising:

prior to receiving the NRZ data stream, receiving predetermined training data;

determining first bit values from the training data;

correcting the determined first bit values with the predetermined training data; and,

using the corrections of the first bit values to adjust the first, second, and third threshold values.

17. (Currently Amended) A non-causal channel equalization communication system, the system comprising:

a multi-threshold decision circuit having an input to accept a non-return to zero (NRZ) data stream, an input to accept threshold values, and outputs to provide bit estimates responsive to a plurality of voltage threshold levels; and,

a non-causal circuit having inputs to accept bit estimates from the multi-threshold decision circuit, the non-causal circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles, the non-causal circuit having an output to supply a bit value

for the current bit estimate determined in response to ~~the~~ non-causal bit value comparisons.

18. (Currently Amended) The system of claim 17 wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs, the future decision circuit having outputs to supply ~~the current,~~ a first bit[[,]] estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimate, the third bit value, and a second bit value, the present decision circuit comparing the first bit estimate to both the second bit value, received prior to the first bit estimate, and the third bit value, received subsequent to the first bit estimate, the present decision circuit having an output to supply a ~~the~~ first bit value determined in response to comparing the first bit estimates to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.

19. (Original) The system of claim 18 wherein the multi-threshold circuit includes:

a first comparator having an input to accept the NRZ data stream, an input establishing a first threshold (V1), and an output to supply a signal distinguishing when the NRZ data stream input has a high probability of being a “1” bit value;

a second comparator having an input to accept the NRZ data stream, an input establishing a second threshold (V0), and an output to

supply a signal distinguishing when the NRZ data stream input has a high probability of being a "0" bit value; and,

a third comparator having an input to accept the NRZ data stream, an input establishing a third threshold (Vopt), and an output to provide a signal when the NRZ data stream input has an approximately equal probability of being a "0" value as a "1" value.

20. (Original) The system of claim 19 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input below the third threshold and above the second threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "1" if both the second and third bit value are "0" values;

a first bit value of "0" if only one of the second and third bit values is a "0" value; and,

a first bit value of "0" if both the second and third bit values are a "1".

21. (Original) The system of claim 20 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input above the third threshold and below the first threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "0" if both the second and third bit value are "1" values;

a first bit value of "1" if only one of the second and third bit values is a "1" value; and,

a first bit value of "1" if both the second and third bit values are a "0".

22. (Currently Amended) The system of claim 21 wherein the multi-threshold circuit accepts an NRZ data stream encoded with forward error correction (FEC); and,

the system further comprising:

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding, the FEC circuit having an output to supply threshold values to the multi-threshold circuit in response to ~~the~~ FEC corrections and an output to supply a stream of corrected data bits.

23. (Currently Amended) The system of claim 22 wherein the FEC circuit includes a first threshold generator having an inputs to accept the first bit value[[s]] from the non-causal circuit and the stream of corrected data bits <u>from the FEC circuit</u>, the first threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "1" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "1" values; and,

wherein the first threshold generator has an output to supply the first threshold (V1) in response to corrections tracked when the second and third bits are both "1" values.

24. (Currently Amended) The system of claim 23 wherein the FEC circuit includes a second threshold generator having inputs to accept the first bit value[[s]] from the non-causal circuit and the stream of corrected data bits <u>from the FEC circuit</u>, the second threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "0" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "0" values; and,

wherein the second threshold generator has an output to supply the second threshold (V0) in response to corrections tracked when the second and third bits are both "0" values.

25. (Currently Amended) The system of claim 24 wherein the FEC circuit includes a third threshold generator having inputs to accept the first bit value[[s]] from the non-causal circuit and the stream of corrected data bits <u>from the FEC circuit</u>, the third threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and only one of the second and third bits is a "1" value; and,

wherein the third threshold generator has an output to supply the third threshold (Vopt) in response to corrections tracked in the first bit when one of the second or third bit values is a "1" value.

26. (Currently Amended) The system of claim 24 wherein the FEC circuit includes a third threshold generator having inputs to accept the first bit value[[s]] from the non-causal circuit and the stream of corrected data bits <u>from the FEC circuit</u>, the third threshold generator tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and adjusting the third threshold (Vopt) in response to corrections tracked when the first bit is determined to be a "1" value.

27. (Original) The system of claim 21 further comprising:

a first threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data stream, the first threshold generator tracking the NRZ data stream inputs when the second and third bit values both equal "1" and maintaining a long-term average of the tracked NRZ data stream inputs, the first threshold generator having an output to supply the first threshold (V1) responsive to the long-term average.

28. (Original) The system of claim 27 further comprising:

a second threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data

stream input, the second threshold generator tracking the NRZ data stream inputs when the second and third bit values both equal "0" and maintaining a long-term average of the NRZ data stream inputs, the second threshold generator having an output to supply the second threshold (V0) responsive to the long-term average.

29. (Original) The system of claim 28 further comprising:

a third threshold generator having inputs to accept the first (V1) and second (V0) thresholds, and an output to supply the third threshold (Vopt) responsive to the first and second thresholds.

30. (Original) The system of claim 29 wherein the third threshold generator supplies the third threshold approximately midway between the first and second thresholds.

31. (Original) The system of claim 28 further comprising:

a third threshold generator having an input to accept the NRZ data stream input, the third threshold generator measuring the average voltage of the NRZ data stream and supplying the third threshold (Vopt) at an output in response to the measured average.

32. (Original) The system of claim 21 wherein the multi-threshold circuit receives NRZ training data input;

wherein the non-causal circuit supplies first bit values responsive to the received NRZ training data; and,

the system further comprising:

a training circuit with a memory including predetermined training data, an input to accept the first bit values from the non-causal circuit, the training circuit comparing the received first bit values to the training data in memory, and supplying first, second, and third threshold values at an output in response to the comparisons.

33. (New) A non-causal channel equalization communication system, the system comprising:

a multi-threshold decision circuit having an input to accept a data stream and outputs to provide bit estimates responsive to a plurality of voltage threshold levels; and,

a non-causal circuit having an input to accept bit estimates from the multi-threshold decision circuit, the non-causal circuit comparing a current bit estimate to bit values supplied across a plurality of clock cycles, the non-causal circuit having an output to supply a bit value for the current bit estimate.

34. (New) The system of claim 33 wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs, the future decision circuit having outputs to supply a first bit estimate and subsequent bit values;

a present decision circuit having inputs to accept the first bit estimate, the subsequent bit values, and prior bit values, the present decision circuit comparing the first bit estimate to both the prior bit values, received prior to the first bit estimate, and the subsequent bit

values, received subsequent to the first bit estimate, the present decision circuit having an output to supply a first bit value determined in response to comparing the first bit estimate to the prior and subsequent bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the prior bit values.

35. (New) A non-causal channel equalization communication system, the system comprising:

a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction and an output to provide bit estimates responsive to a plurality of voltage threshold levels;

a non-causal circuit having an input to accept bit estimates from the multi-threshold decision circuit, the non-causal circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles, the non-causal circuit having an output to supply a bit value for the current bit estimate; and,

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the data stream and correcting first bit values in response to the decoding, the FEC circuit having an output to supply threshold levels to the multi-threshold circuit in response to the FEC corrections.

36. (New) The system of claim 35 wherein the non-causal circuit includes:

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a future decision circuit having inputs connected to the mutli-threshold circuit outputs, the future decision circuit having outputs to supply a first bit estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimate, the third bit value, and a second bit value, the present decision circuit comparing the first bit estimate to both the second bit value, received prior to the first bit estimate, and the third bit value, received subsequent to the first bit estimate, the present decision circuit having an output to supply a first bit value determined in response to comparing the first bit estimates to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.